CLAIMS

What is claimed is:

1. A method of transmission power control for a wireless transmit receive unit (WTRU) that transmits data signals in a forward channel in selectively sized block allocations where the WTRU is configured to make forward channel power adjustments as a function of target metrics computed based on the data signals as received over the forward channel, the method comprising:

receiving data signals from the WTRU in a block allocation having a predetermined size S on the forward channel;

computing target metrics for the WTRU's forward channel power adjustments based on the detection of predetermined error conditions in the signals received on the forward channel including:

setting an initial target metric value; and

after a preliminary period at the initial value, changing the target metric by a step up or a step down amount at time intervals of a predetermined length whereby the target metric is increased by the step up amount if a predetermined error condition has been detected in an immediately preceding time interval or is decreased by the step down amount if the predetermined error condition has not been detected the immediately preceding time interval; and

setting the step down amount at an initial transient state level based on the predetermined block allocation size S, such that the initial step down amount is set at a level at least as great as a predetermined step down amount for a steady state steady state level and, where the initial step down amount is greater than the predetermined step down amount for the steady state steady state level, reducing the step down amount by a selected amount to a lower level if a predetermined error condition has been detected in an immediately preceding time interval until the step down amount is reduced to the predetermined step down amount for the steady state steady state level.

2. The method of claim 1 where the step up amount has a defined correspondence with the step down amount for each level wherein the computing

target metrics further includes increasing the step up and step down amounts by a selected amount if a predetermined error condition has not been detected in a predetermined number of time intervals while the step down amount is set at the steady state level.

3. The method of claim 1 where the step up amount has a defined correspondence with the step down amount for each level, the target metrics are target signal to interference ratios (SIRs) and cyclic redundancy checks are conducted to detect the predetermined error condition.

4. The method of claim 3 wherein step up amounts are significantly greater than respective step down amounts, the initial transient level step down amount is a factor of 2^n of the predetermined step down amount for the steady state steady state level, where n is non-negative integer, and where the step down amount is reduced, reduction is by a factor of 1/2.

5. The method of claim 4 wherein the computing target metrics further includes increasing the step up and step down amounts by a factor of 2 if a predetermined error condition has not been detected in a predetermined number of time intervals while the step down amount is set at the steady state level.

6. The method of claim 4 wherein block allocation sizes S are defined in increments of Transmission Time Intervals (TTIs) and the initial step down amount is set such that n=0 for S <100 TTIs, n=1 for 100 TTIs $\leq$ S < 200 TTIs, n=2 for 200 TTIs $\leq$ S < 400 TTIs and n=3 for S $\geq$ 400 TTIs.

7. The method of claim 6 wherein the method is implemented in a Universal Mobile Telecommunications System (UMTS) where the WTRU is a network unit that transmits user signals on a downlink channel and the computing of target metrics is performed by a WTRU that receives the downlink channel and

produces power step commands that are transmitted to the network unit on an uplink channel.

8. The method of claim 3 wherein the WTRU is a network unit that transmits user signals on a downlink channel and the computing of target metrics is performed by a WTRU that receives the downlink channel.

9. The method of claim 3 wherein the WTRU transmits user signals on an uplink channel and the computing of target metrics is performed by a network unit that receives the uplink channel.

10. The method of claim 3 in which open loop transmission power control for the WTRU is implemented further comprising receiving the computed target SIRs by the WTRU on a reverse channel such that the WTRU computes power adjustments for forward channel transmissions based on received target SIRs.

11. The method of claim 3 in which closed loop transmission power control for the WTRU is implemented further comprising:

producing power step commands as a function of the computed target SIRs and transmitting the power step commands on a reverse channel; and

receiving the power step commands by the WTRU on the reverse channel and computing power adjustments for forward channel transmissions based on the received power step commands.

12. A receiving wireless transmit receive unit (WTRU) for implementing transmission power control for a transmitting WTRU that transmits data signals in a forward channel in selectively sized block allocations where the transmitting WTRU is configured to make forward channel transmission power adjustments as a function of target metrics computed by the receiving WTRU, the receiving WTRU comprising:

a receiver for receiving data signals in a block allocation having a predetermined size S from a transmitting WTRU on a forward channel;

a processor for computing target metrics for implementing forward channel transmission power adjustments in the transmitting WTRU based on the detection of predetermined error conditions in the data signals received on the forward channel; and

said processor configured to compute target metrics such that:

after a preliminary period at an initial value, the target metric is changed by a step up or a step down amount at time intervals of a predetermined length whereby the target metric is increased by the step up amount if a predetermined error condition has been detected in an immediately preceding time interval or the target metric is decreased by the step down amount if the predetermined error condition has not been detected in the immediately preceding time interval;

the step down amount is set at an initial transient state level based on the predetermined block allocation size S, such that the initial step down amount is set at a level at least as great as a predetermined step down amount for a steady state steady state level; and

where the initial step down amount is greater than the predetermined step down amount for the steady state steady state level, the step down amount is reduced by a selected amount to a lower level if a predetermined error condition has been detected in an immediately preceding time interval until the step down amount is reduced to the predetermined step down amount for the steady state steady state level.

13. The invention of claim 12 wherein said processor is further configured to compute target metrics such that the step up amount has a defined correspondence with the step down amount for each level and the step up and step down amounts are increased by a selected amount if a predetermined error condition has not been detected in a predetermined number of time intervals while the step down amount is set at the steady state level.

14. The invention of claim 12 in which the target metrics are target signal to interference ratios (SIRs) wherein said processor is further configured to compute target metrics such that the step up amount has a defined correspondence with the step down amount for each level and the receiving WTRU is configured to conduct cyclic redundancy checks to detect the predetermined error condition.

15. The invention of claim 14 wherein said processor is configured to compute target metrics such that step up amounts are significantly greater than respective step down amounts, the initial transient level step down amount is a factor of 2^n of the predetermined step down amount for the steady state steady state level, where n is non-negative integer, and where the step down amount is reduced, reduction is by a factor of 1/2.

16. The invention of claim 15 wherein said processor is further configured to compute target metrics such that the step up and step down amounts are increased by a factor of 2 if a predetermined error condition has not been detected in a predetermined number of time intervals while the step down amount is set at the steady state level.

17. The invention of claim 15 wherein block allocation sizes S are defined in increments of Transmission Time Intervals (TTIs) and said processor is further configured to compute target metrics such that the initial step down amount is set such that $n=0$ for $S <100$ TTIs, $n=1$ for 100 TTIs $\leq S <$ 200 TTIs, $n=2$ for 200 TTIs $\leq S <$ 400 TTIs and $n=3$ for $S \geq$ 400 TTIs.

18. The invention of claim 17 which is implemented for use in a Universal Mobile Telecommunications System (UMTS) where the WTRU is a network unit that transmits user signals on a downlink wherein the receiving WTRU is configured to compute target metrics based on the detection of predetermined error conditions in the data signals received on the downlink channel.

19. The invention of claim 14 where the transmitting WTRU is a network unit that transmits user signals on a downlink channel wherein the receiving WTRU is configured to compute target metrics based on the detection of predetermined error conditions in the data signals received on the downlink channel.

20. The invention of claim 14 where the transmitting WTRU transmits user signals on an uplink channel wherein the receiving WTRU is configured to compute target metrics based on the detection of predetermined error conditions in the data signals received on the uplink channel.

21. The invention of claim 14 in which open loop transmission power control for the transmitting WTRU is implemented wherein the receiving WTRU further comprising a transmitter configured to transmit the computed target SIRs on a reverse channel to the transmitting WTRU.

22. The invention of claim 14 in which closed loop transmission power control for the transmitting WTRU is implemented wherein the receiving WTRU processor is further configured to produce power step commands as a function of the computed target SIRs and the receiving WTRU further comprising a transmitter configured to transmit the power step commands on a reverse channel to the transmitting WTRU.

23. A method of transmission power control for a wireless transmit receive unit (WTRU) that transmits data signals in a forward channel in selectively sized block allocations where the WTRU is configured to make forward channel power adjustments as a function of target metrics computed based on the data signals as received over the forward channel, the method comprising:

receiving a series of block allocations of data signals spaced apart in time from the WTRU on the forward channel;

for the data signals of each block allocation, computing target metrics for the WTRU's forward channel power adjustments based on the detection of predetermined error conditions in the signals received on the forward channel including setting an initial target metric value and storing a last target metric computed for each block allocation of data; and

for the data signals of each block allocation after a first block allocation, setting the initial target metric value as a function of the last target metric computed for an immediately preceding block allocation and an inter-allocation adjustment based on the time spacing from the immediately preceding block allocation.

24. The method of claim 23 where each the block allocation has a predetermined size S wherein the computing target metrics for the WTRU's forward channel power adjustments based on the detection of predetermined error conditions in the signals received on the forward channel further includes:

after a preliminary period at the initial value, changing the target metric by a step up or a step down amount at time intervals of a predetermined length whereby the target metric is increased by the step up amount if a predetermined error condition has been detected in an immediately preceding time interval or is decreased by the step down amount if the predetermined error condition has not been detected the immediately preceding time interval; and

setting the step down amount at an initial transient state level based on the predetermined block allocation size S, such that the initial step down amount is set at a level at least as great as a predetermined step down amount for a steady state steady state level and, where the initial step down amount is greater than the predetermined step down amount for the steady state steady state level, reducing the step down amount by a selected amount to a lower level if a predetermined error condition has been detected in an immediately preceding time interval until the step down amount is reduced to the predetermined step down amount for the steady state steady state level.

25. The method of claim 23 wherein the inter-allocation adjustment is determined by (alpha*previous_target_SIR)+((1-alpha)*initial_target_SIR)), where alpha is a forgetting factor to compensate for longer than expected inter-allocation time, previous_target_SIR is the target metric from the previous block allocation, and initial_target_SIR is the first target metric.

26. The method of claim 23 further comprising an upper and lower bound test for setting the initial target metric, where the upper bound is a first predetermined value added to the initial value and the lower bound is a second predetermined value subtracted from the initial value.

27. The method of claim 23 further comprising an adjustment to the target metric based on data rate.

28. The method of claim 23 where the step up amount has a defined correspondence with the step down amount for each level, the target metrics are target signal to interference ratios (SIRs) and cyclic redundancy checks are conducted to detect the predetermined error condition.

29. The method of claim 28 wherein step up amounts are significantly greater than respective step down amounts, the initial transient level step down amount is a factor of 2^n of the predetermined step down amount for the steady state steady state level, where n is non-negative integer, and where the step down amount is reduced, reduction is by a factor of 1/2.

30. The method of claim 29 wherein the computing target metrics further includes increasing the step up and step down amounts by a factor of 2 if a predetermined error condition has not been detected in a predetermined number of time intervals while the step down amount is set at the steady state level.

31. The method of claim 29 wherein block allocation sizes S are defined in increments of Transmission Time Intervals (TTIs) and the initial step down amount is set such that n=0 for S <100 TTIs, n=1 for 100 TTIs ≤ S < 200 TTIs, n=2 for 200 TTIs ≤ S < 400 TTIs and n=3 for S ≥ 400 TTIs.

32. The method of claim 31 wherein the method is implemented in a Universal Mobile Telecommunications System (UMTS) where the WTRU is a network unit that transmits user signals on a downlink channel and the computing of target metrics is performed by a WTRU that receives the downlink channel and produces power step commands that are transmitted to the network unit on an uplink channel.

33. The method of claim 28 wherein the WTRU is a network unit that transmits user signals on a downlink channel and the computing of target metrics is performed by a WTRU that receives the downlink channel.

34. The method of claim 28 wherein the WTRU transmits user signals on an uplink channel and the computing of target metrics is performed by a network unit that receives the uplink channel.

35. The method of claim 28 in which open loop transmission power control for the WTRU is implemented further comprising receiving the computed target SIRs by the WTRU on a reverse channel such that the WTRU computes power adjustments for forward channel transmissions based on received target SIRs.

36. A receiving wireless transmit receive unit (WTRU) for implementing transmission power control for a transmitting WTRU that transmits data signals in a forward channel in selectively sized block allocations where the transmitting WTRU is configured to make forward channel transmission power adjustments as a

function of target metrics computed by the receiving WTRU, the receiving WTRU comprising:

a receiver for receiving a series of block allocations of data signals spaced apart in time from the WTRU on the forward channel;

a processor for computing target metrics for implementing forward channel transmission power adjustments in the transmitting WTRU based on the detection of predetermined error conditions in the data signals received on the forward channel; and

said processor configured to compute target metrics such that:

for the data signals of each block allocation, an initial target metric value is set and a last target metric computed for each block allocation of data is stored; and

for the data signals of each block allocation after a first block allocation, the initial target metric value is set as a function of the stored last target metric computed for an immediately preceding block allocation and the time spacing from the immediately preceding block allocation.

37. The invention of claim 36 where each block allocation has a predetermined size S wherein said processor is further configured to compute target metrics such that:

after a preliminary period at an initial value, the target metric is changed by a step up or a step down amount at time intervals of a predetermined length whereby the target metric is increased by the step up amount if a predetermined error condition has been detected in an immediately preceding time interval or the target metric is decreased by the step down amount if the predetermined error condition has not been detected in the immediately preceding time interval;

the step down amount is set at an initial transient state level based on the predetermined block allocation size S, such that the initial step down amount is set at a level at least as great as a predetermined step down amount for a steady state steady state level; and

where the initial step down amount is greater than the predetermined step down amount for the steady state steady state level, the step down amount is reduced by a selected amount to a lower level if a predetermined error condition has been detected in an immediately preceding time interval until the step down amount is reduced to the predetermined step down amount for the steady state steady state level.

38. The invention of claim 36 wherein the inter-allocation adjustment is determined by (alpha*previous_target_SIR)+((1-alpha)*initial_target_SIR)), where alpha is a forgetting factor to compensate for longer than expected inter-allocation time, previous_target_SIR is the target metric from the previous block allocation, and initial_target_SIR is the first target metric.

39. The invention of claim 36 wherein the processor is further configured to perform an upper and lower bound test for setting the initial target metric, where the upper bound is a first predetermined value added to the initial value and the lower bound is a second predetermined value subtracted from the initial value.

40. The invention of claim 36 wherein the processor is further configured to adjust the target metric based on data rate.

41. The invention of claim 36 in which the target metrics are target signal to interference ratios (SIRs) wherein said processor is further configured to compute target metrics such that the step up amount has a defined correspondence with the step down amount for each level and the receiving WTRU is configured to conduct cyclic redundancy checks to detect the predetermined error condition.

42. The invention of claim 41 wherein said processor is configured to compute target metrics such that step up amounts are significantly greater than respective step down amounts, the initial transient level step down amount is a factor of 2^n of the predetermined step down amount for the steady state steady state

level, where n is non-negative integer, and where the step down amount is reduced, reduction is by a factor of 1/2.

43. The invention of claim 42 wherein said processor is further configured to compute target metrics such that the step up and step down amounts are increased by a factor of 2 if a predetermined error condition has not been detected in a predetermined number of time intervals while the step down amount is set at the steady state level.

44. The invention of claim 42 wherein block allocation sizes S are defined in increments of Transmission Time Intervals (TTIs) and said processor is further configured to compute target metrics such that the initial step down amount is set such that n=0 for $S < 100$ TTIs, n=1 for 100 TTIs $\leq S <$ 200 TTIs, n=2 for 200 TTIs $\leq$ $S <$ 400 TTIs and n=3 for $S \geq$ 400 TTIs.

45. The invention of claim 44 which is implemented for use in a Universal Mobile Telecommunications System (UMTS) where the WTRU is a network unit that transmits user signals on a downlink wherein the receiving WTRU is configured to compute target metrics based on the detection of predetermined error conditions in the data signals received on the downlink channel.

46. The invention of claim 41 where the transmitting WTRU is a network unit that transmits user signals on a downlink channel wherein the receiving WTRU is configured to compute target metrics based on the detection of predetermined error conditions in the data signals received on the downlink channel.

47. The invention of claim 41 where the transmitting WTRU transmits user signals on an uplink channel wherein the receiving WTRU is configured to compute target metrics based on the detection of predetermined error conditions in the data signals received on the uplink channel.

48. The invention of claim 41 in which open loop transmission power control for the transmitting WTRU is implemented wherein the receiving WTRU further comprises a transmitter configured to transmit the computed target SIRs on a reverse channel to the transmitting WTRU.

49. The invention of claim 41 in which closed loop transmission power control for the transmitting WTRU is implemented wherein the receiving WTRU processor is further configured to produce power step commands as a function of the computed target SIRs and the receiving WTRU further comprising a transmitter configured to transmit the power step commands on a reverse channel to the transmitting WTRU.